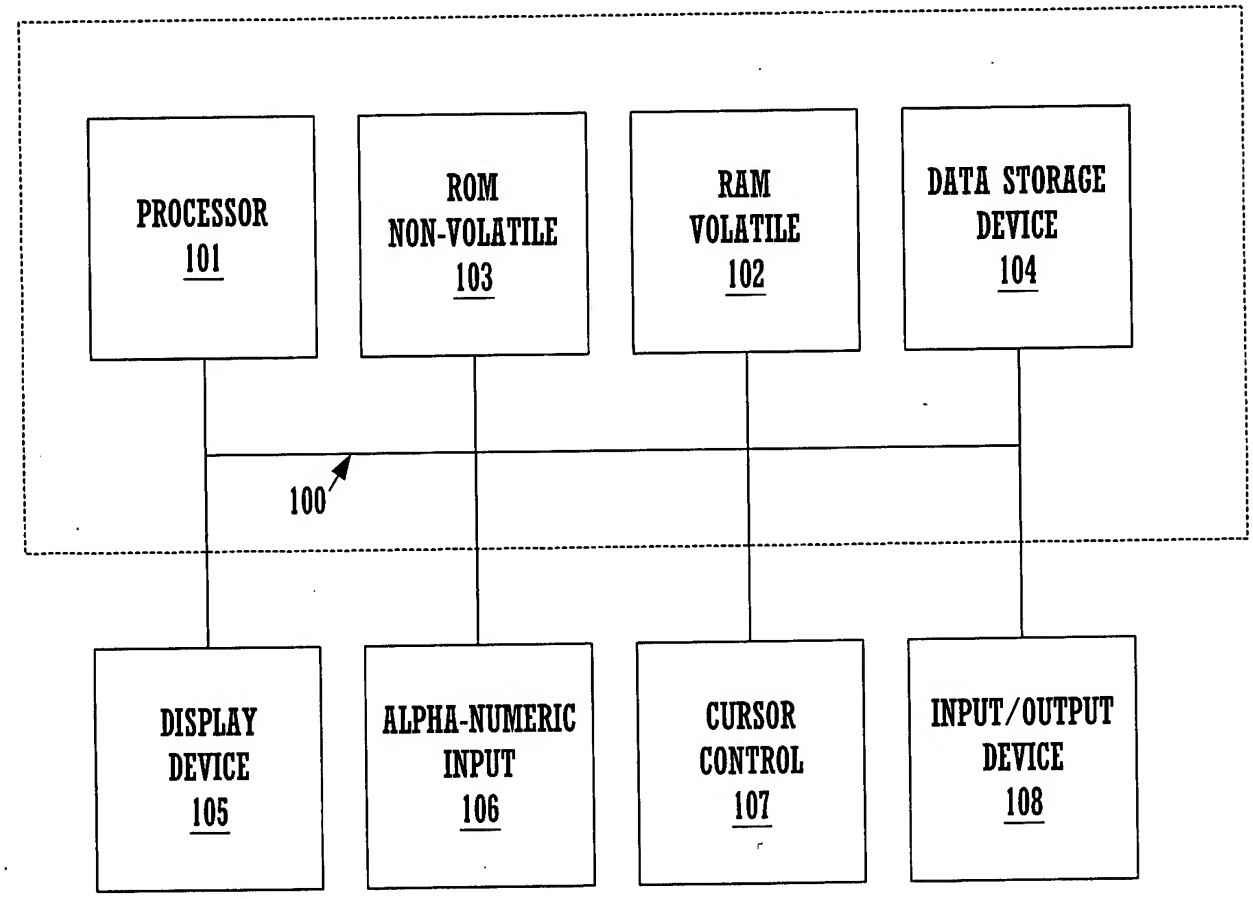

FIGURE 1

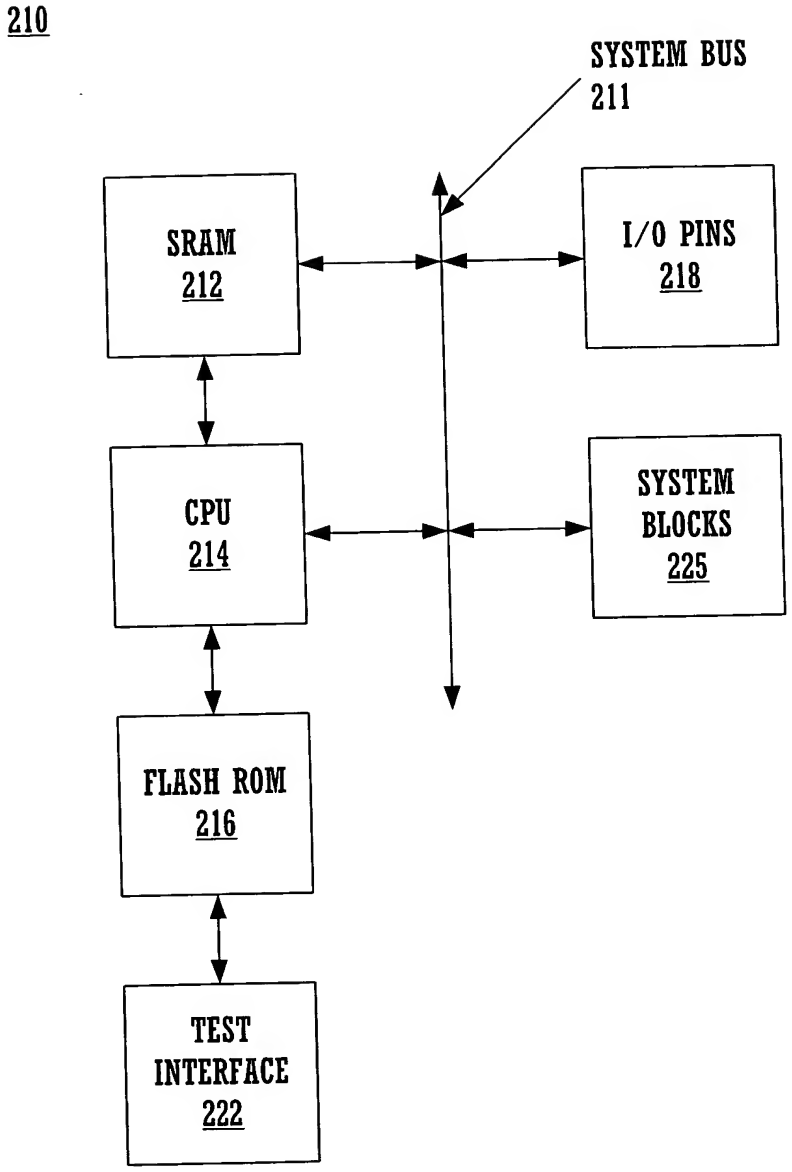
210
SYSTEM BUS
211
SRAM
212
I/O PINS
218
CPU
214
SYSTEM
BLOCKS
225
FLASH ROM
216
TEST
INTERFACE
222

FIGURE 2A

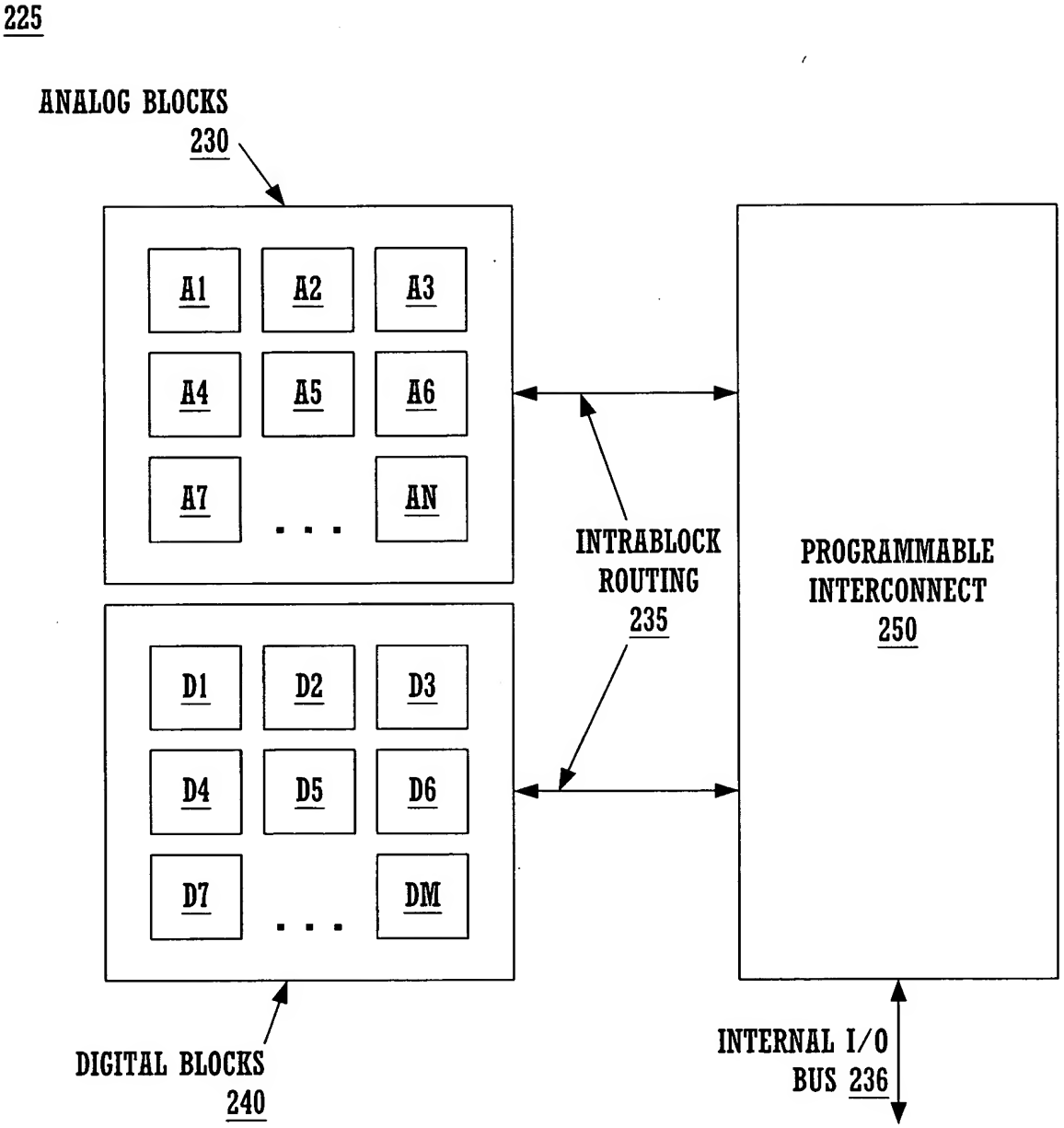
225
ANALOG BLOCKS
230
A1
A2
A3
A4
A5
A6
A7
AN
D1
D2
D3
D4
D5
D6
D7
DM
INTRABLOCK
ROUTING
235
PROGRAMMABLE
INTERCONNECT
250
DIGITAL BLOCKS
240
INTERNAL I/O
BUS 236

FIGURE 2B

300

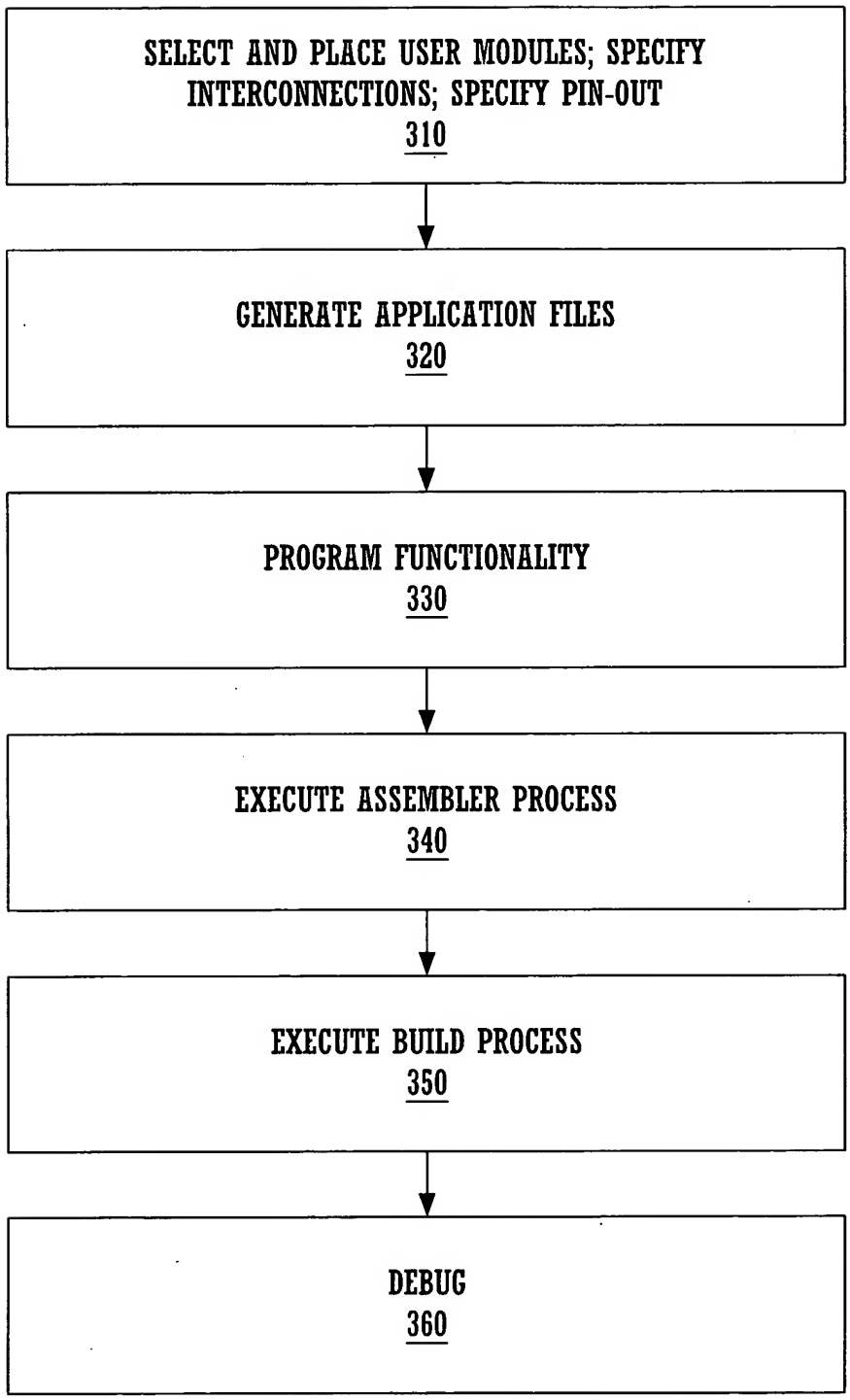
SELECT AND PLACE USER MODULES; SPECIFY INTERCONNECTIONS; SPECIFY PIN-OUT
310
GENERATE APPLICATION FILES
320
PROGRAM FUNCTIONALITY
330
EXECUTE ASSEMBLER PROCESS
340
EXECUTE BUILD PROCESS
350
DEBUG
360

FIGURE 3

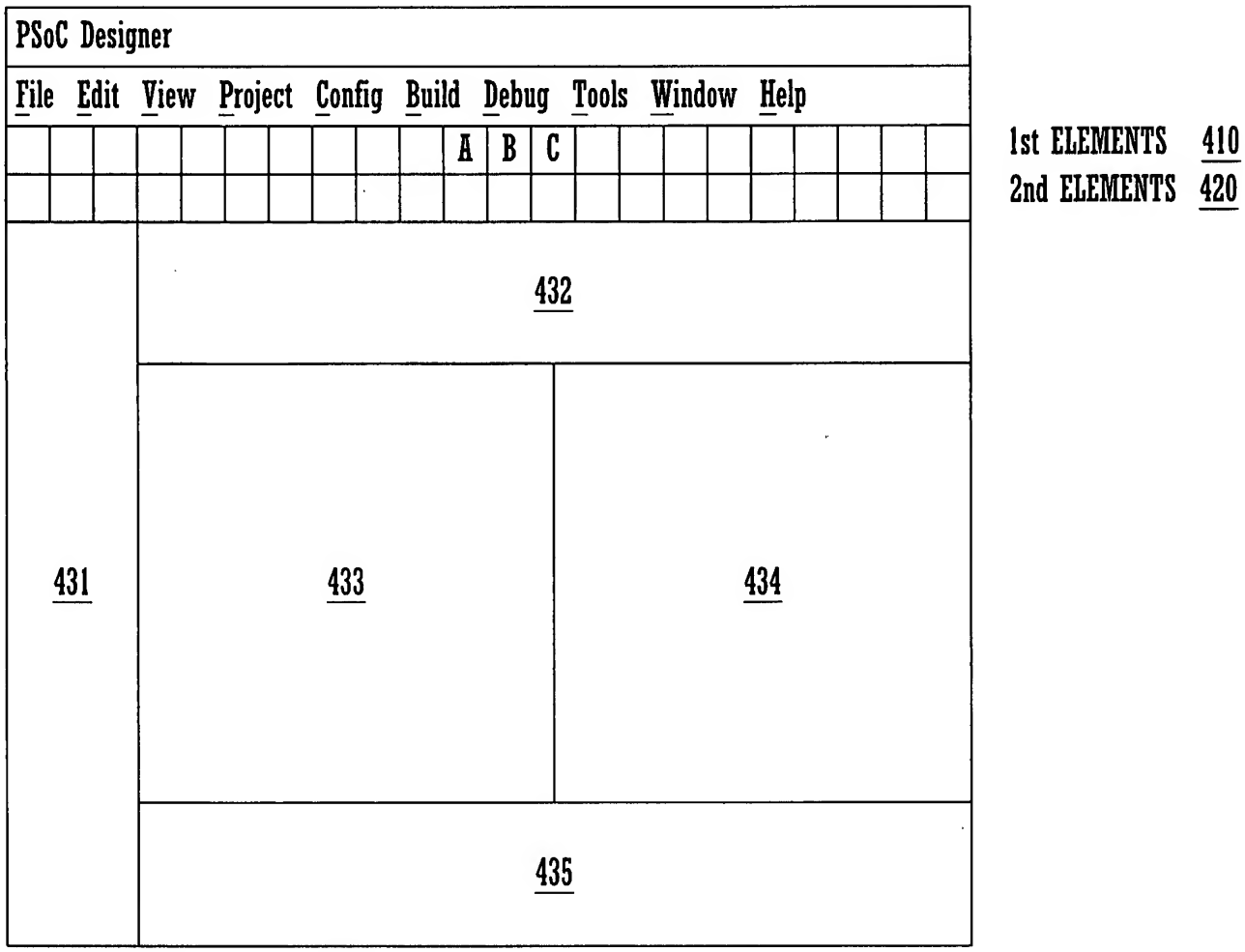
400
PSoC Designer
File Edit View Project Config Build Debug Tools Window Help
A B C
1st ELEMENTS 410
2nd ELEMENTS 420
432
431
433
434
435

FIGURE 4A

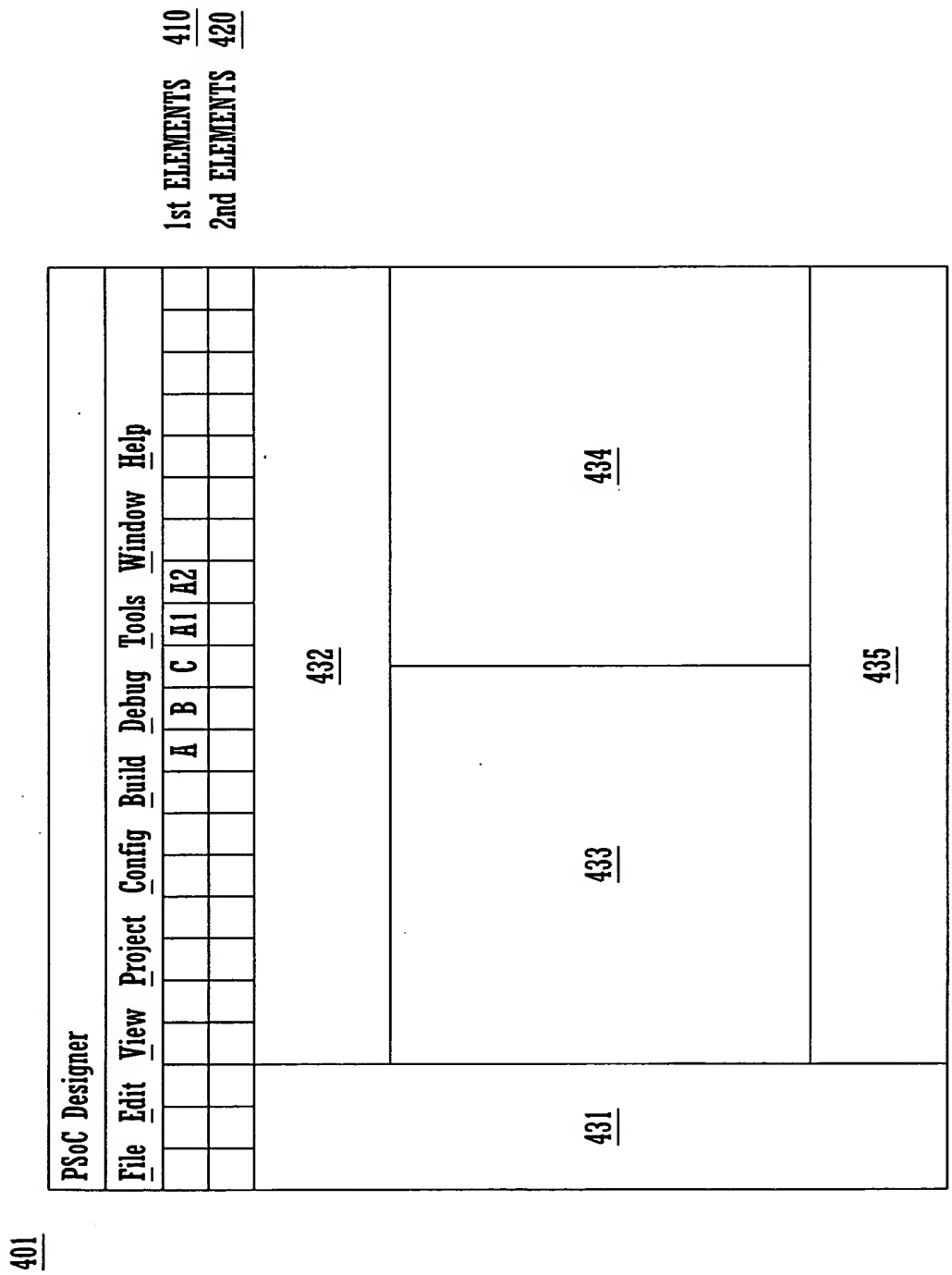
401
PSoC Designer
File Edit View Project Config Build Debug Tools Window Help
A B C A1 A2
1st ELEMENTS 410
2nd ELEMENTS 420
431
432
433
434
435

FIGURE 4B

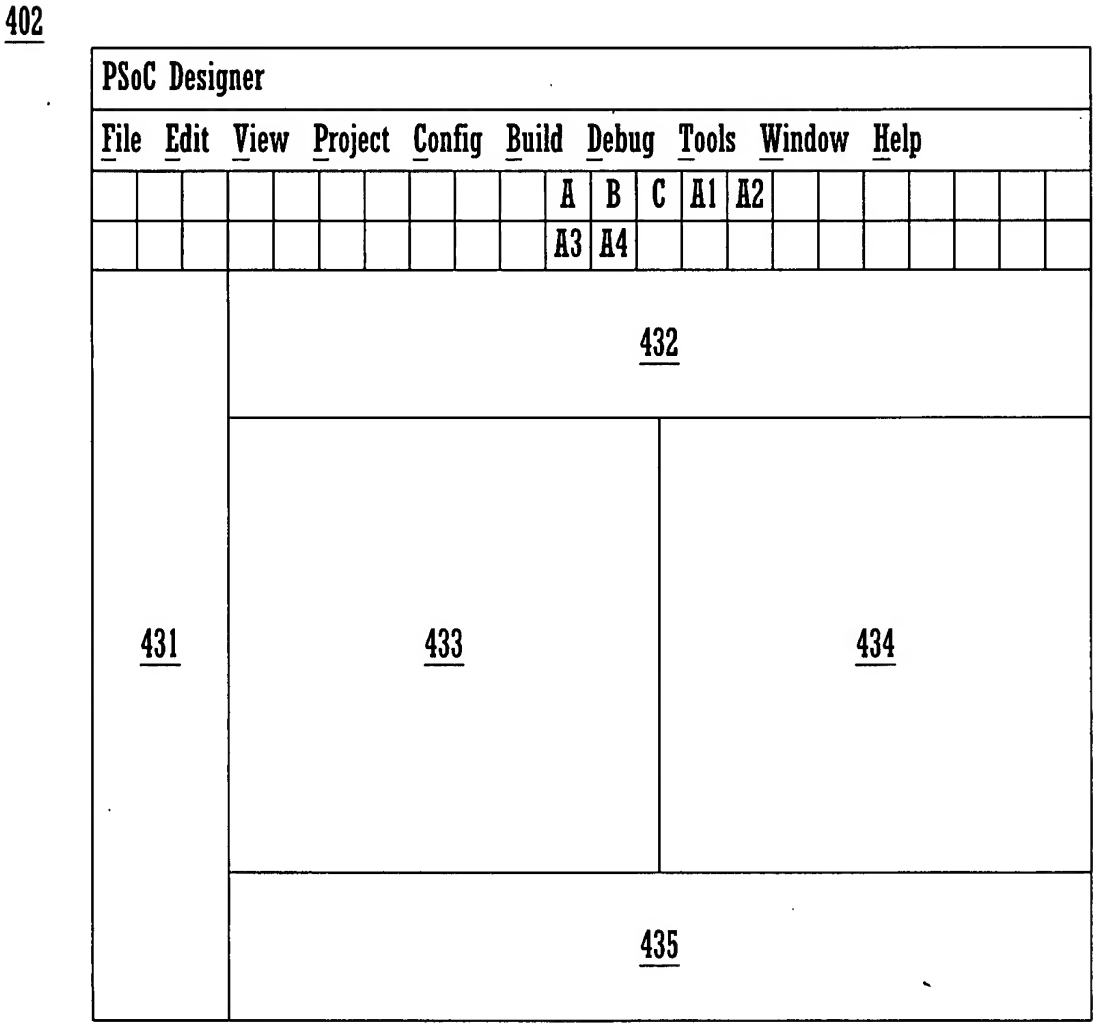
402
PSoC Designer
File Edit View Project Config Build Debug Tools Window Help
A B C A1 A2
A3 A4
1st ELEMENTS 410
2nd ELEMENTS 420
432
431
433
434
435

FIGURE 4C

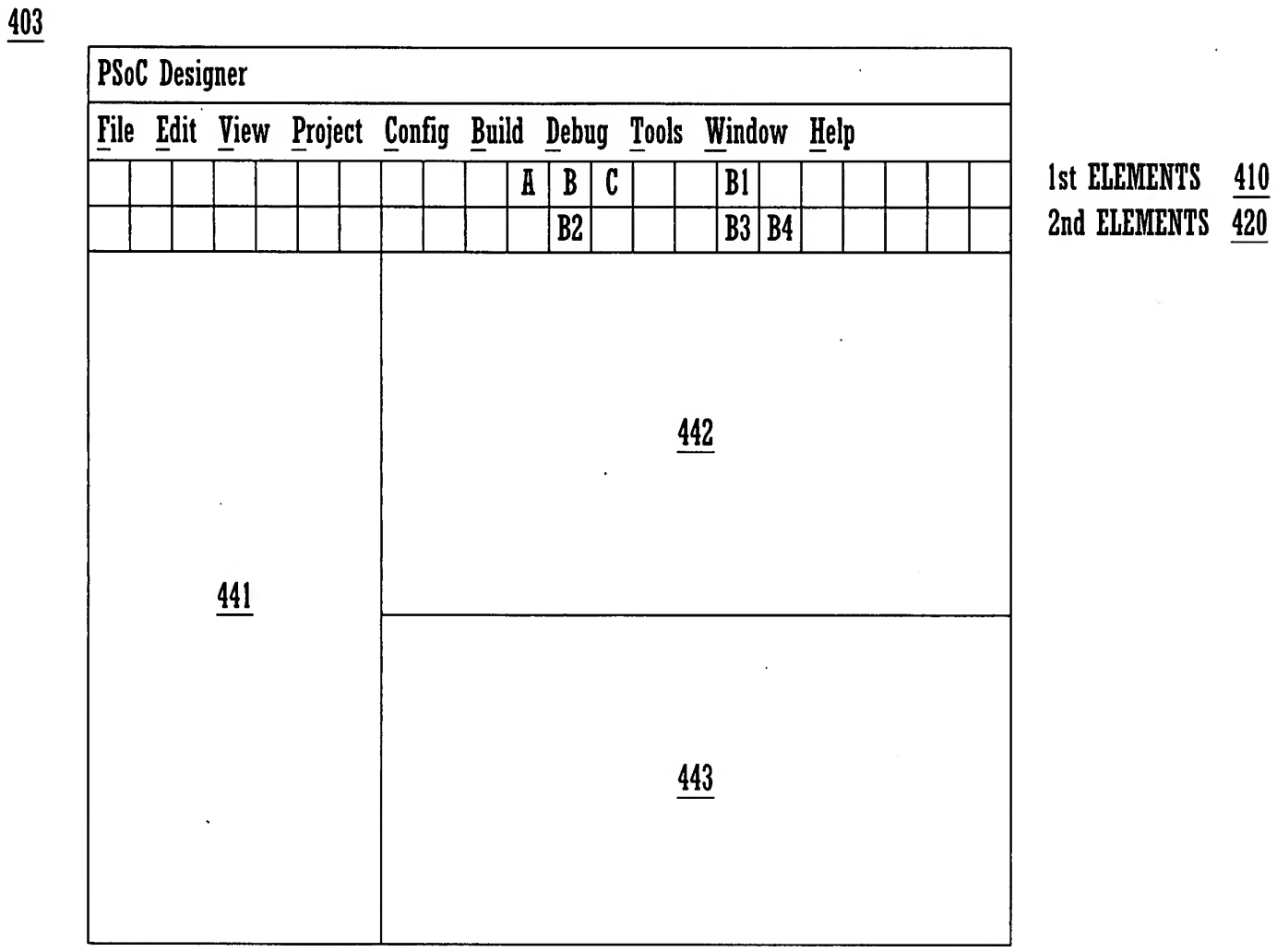
403
PSoC Designer
File Edit View Project Config Build Debug Tools Window Help
A B C B1
B2 B3 B4
1st ELEMENTS 410
2nd ELEMENTS 420
441
442
443

FIGURE 4D

500

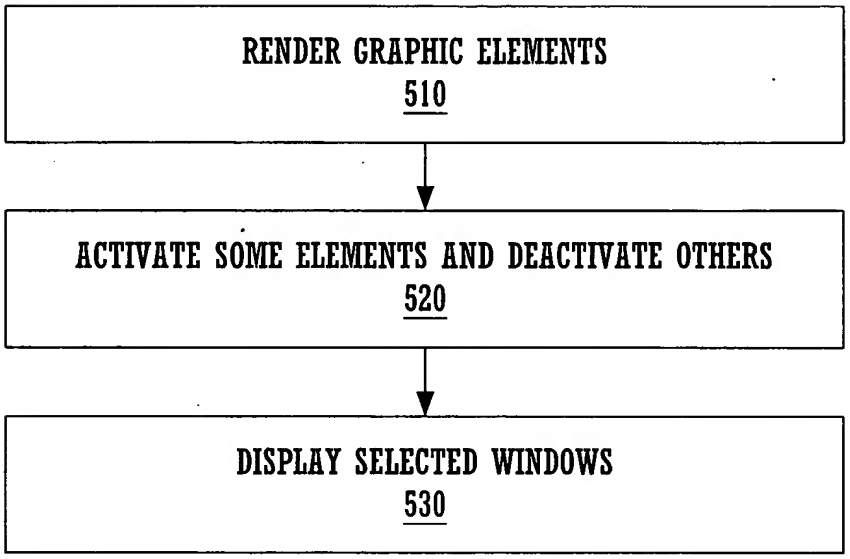
RENDER GRAPHIC ELEMENTS
510
ACTIVATE SOME ELEMENTS AND DEACTIVATE OTHERS
520
DISPLAY SELECTED WINDOWS
530

FIGURE 5

600

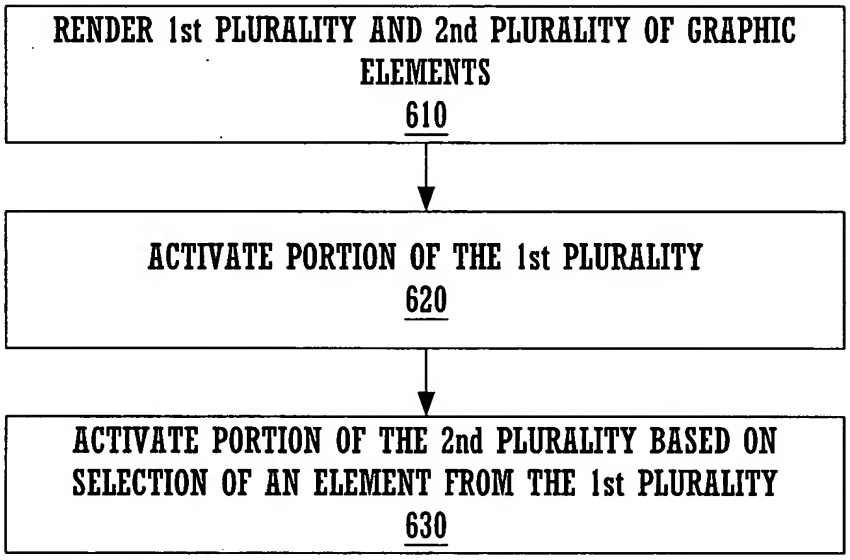
RENDER 1st PLURALITY AND 2nd PLURALITY OF GRAPHIC ELEMENTS
610
ACTIVATE PORTION OF THE 1st PLURALITY
620
ACTIVATE PORTION OF THE 2nd PLURALITY BASED ON SELECTION OF AN ELEMENT FROM THE 1st PLURALITY
630

FIGURE 6

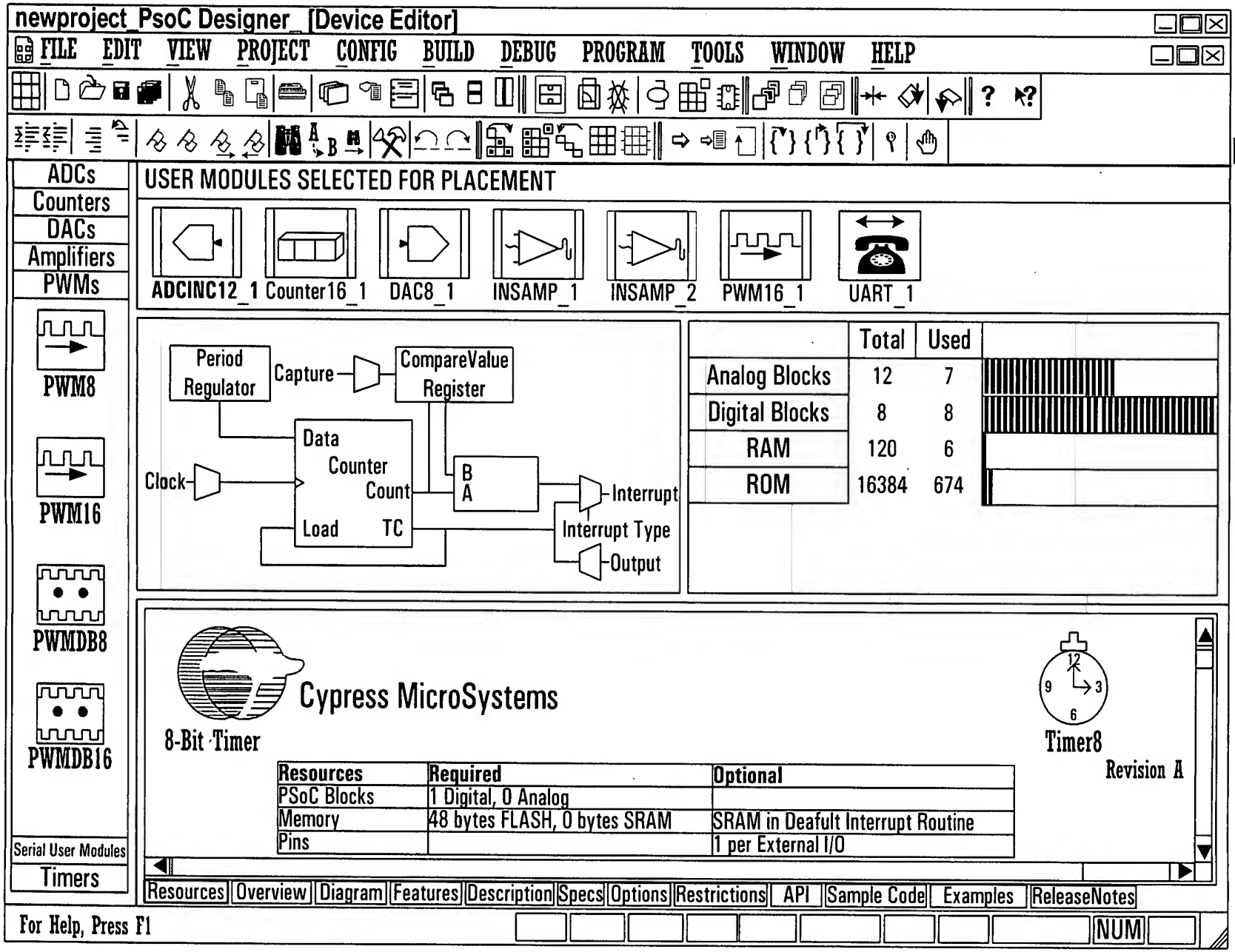
newproject_PsoC Designer_[Device Editor]
FILE EDIT VIEW PROJECT CONFIG BUILD DEBUG PROGRAM TOOLS WINDOW HELP
700
ADCs
Counters
DACs
Amplifiers
PWMs
PWM8
PWM16
PWMDB8
PWMDB16
Serial User Modules
Timers
USER MODULES SELECTED FOR PLACEMENT
ADCINC12_1
Counter16_1
DAC8_1
INSAMP_1
INSAMP_2
PWM16_1
UART_1
Period Regulator
Capture
CompareValue Register
Data Counter Count
Clock
Load
TC
B
A
Interrupt
Interrupt Type
Output
Total
Used
Analog Blocks 12 7
Digital Blocks 8 8
RAM 120 6
ROM 16384 674
Cypress MicroSystems
8-Bit Timer
Timer8
Revision A
Resources
Required
Optional
PSoC Blocks
1 Digital, 0 Analog
Memory
48 bytes FLASH, 0 bytes SRAM
SRAM in Deafult Interrupt Routine
Pins
1 per External I/O
Resources Overview Diagram Features Description Specs Options Restrictions API Sample Code Examples ReleaseNotes
For Help, Press F1
NUM

FIGURE 7